Statement of Volatility – Dell PowerEdge R220

Dell PowerEdge R220 contains both volatile and non-volatile (NV) components. Volatile components lose their data immediately upon removal of power from the component. Non-volatile components continue to retain their data even after the power has been removed from the component. Components chosen as user-definable configuration options (those not soldered to the motherboard) are not included in the Statement of Volatility. Configuration option information (pertinent to options such as microprocessors, remote access controllers, and storage controllers) is available by component separately. The following NV components are present in the PowerEdge R220 server.

Item	Non-Volatile or Volatile	Quantity	Reference Designator	Size
Planer				
PCH Internal CMOS RAM	Non-Volatile	1	U87	256 Bytes
BIOS SPI Flash	Non-Volatile	1	U86	8 M Bytes
iDRAC SPI Flash	Non-Volatile	1	U2	4 M Bytes
BMC EMMC	Non-Volatile	1	U25	4G Bytes
System CPLD RAM	Non-Volatile	1	U18	1K Bytes
TPM	Non-Volatile	1	U8	8064 Bytes

Item	Type (e.g. Flash PROM, EEPROM)	Can user programs or operating system write data to it during normal operation?	Purpose? (e.g. boot code)
Planer			
PCH Internal CMOS RAM	Battery-backed NVRAM	No	Real-time clock and BIOS configuration settings
BIOS SPI Flash	SPI Flash	Yes	Boot code, system configuration information, UEFI environment, Flash descriptor, ME
iDRAC SPI Flash	SPI Flash	No	iDRAC Uboot (bootloader), server management persistent store (i.e. IDRAC MAC

Item	Type (e.g. Flash PROM, EEPROM)	Can user programs or operating system write data to it during normal operation?	Purpose? (e.g. boot code)
			Address, iDRAC boot variables), lifecycle log cache, virtual planar FRU and EPPID, rac log, System Event Log, JobStore, iDRAC Secure Boot Code,
BMC EMMC	EMMC NAND Flash	No	Operational iDRAC FW, Lifecycle Controller (LC) USC partition, LC service diags, LC OS drivers, USC firmware
System CPLD RAM	RAM	No	Not utilized
TPM	EEPROM	No	Data Protection

Item	How is data input to this memory?	How is this memory write protected?
Planer		
PCH Internal CMOS RAM	BIOS default settings, which can be altered by F2 Setup Menu during POST	Not accessible
BIOS SPI Flash	Loading flash memory requires a vendor-provided firmware file and loader program which is executed by booting up the system from a USB key (or floppy). In addition, an OS-based update package executable containing the firmware file can be run. A system loaded with arbitrary data in BIOS FLASH memory will not operate.	Software write protected
iDRAC SPI Flash	Loading flash memory requires a vendor provided firmware file and loader program. System loaded with arbitrary data in flash memory would not operate.	Software write protected
BMC EMMC	Loading flash memory requires a vendor provided firmware file and loader program which is executed by booting up the system from a floppy or OS-based executable containing	Software write protected

Item	How is data input to this memory?	How is this memory write protected?
	the firmware file and the loader. System loaded with arbitrary data in firmware memory will not operate.	
System CPLD RAM	Not utilized	Not accessible
TPM	Not accessible	Software write protected

Item	How is this memory write protected?	How is the memory cleared?
H310 PERC		
NVSRAM	Not WP. Not visible to Host Processor	Cannot be cleared with existing tools available to the customer
FRU	Not WP	Cannot be cleared with existing tools available to the customer
1-Wire EEPROM	Not WP. Not visible to Host Processor	Cannot be cleared with existing tools available to the customer
SBR	Not WP. Not visible to Host Processor	Cannot be cleared with existing tools available to the customer
Flash	Not WP. Not visible to Host Processor	Cannot be cleared with existing tools available to the customer

NOTE: For any information that you may need, direct your questions to your Dell Marketing contact.